TECHNICAL NOTE

WHAT IS BURST EDO?

INTRODUCTION

Burst Extended Data-Out (BEDO) or pipeline nibble mode (as it has been termed by JEDEC), is basically an EDO DRAM that contains a pipeline stage and a 2-bit burst counter. This evolutionary approach to a high-speed DRAM uses the same signals, packages, SIMMs and DIMMs as the Extended Data-Out (EDO) and Fast Page Mode (FPM) DRAM. Burst EDO is designed as a bond or fuse option on the same die as FPM and EDO devices. This keeps the cost of BEDO the same as FPM and EDO. Micron is implementing the BEDO option on all 16 Meg DRAM die. The organizations are 4 Meg x 4, 2 Meg x 8, and 1 Meg x 16. All Burst EDO DRAMs require V_{CC} to be at 3.3V but the inputs and outputs can interface to both 3.3V and 5V circuits. This 5V-tolerant I/O interface allows the construction of 5V SIMM and DIMM modules by simply placing a voltage regulator on the module.

The difference between BEDO and EDO is that all cycles, READ and WRITE, occur in four-cycle bursts. Longer bursts can be achieved so far as the accesses remain in the same page. Bursts of lengths longer than four, up to the length of a page, are accomplished by providing a new column address on the fifth $\overline{CAS}$ falling edge and then every fourth $\overline{CAS}$ falling edge thereafter. (See Figure 1.)

Burst lengths less than four are accomplished by terminating the burst early. This is done by transitioning the write enable ($\overline{WE}$) signal after the desired data is read or written. Single-cycle accesses are accomplished by transitioning $\overline{WE}$ after the first data is read or written. See Figure 2 for an example of terminating a burst sequence.

Due to the internal pipeline stage, the first falling edge of $\overline{CAS}$ during READ cycles does not produce data as would the EDO DRAM. It takes two $\overline{CAS}$ cycles to produce the first

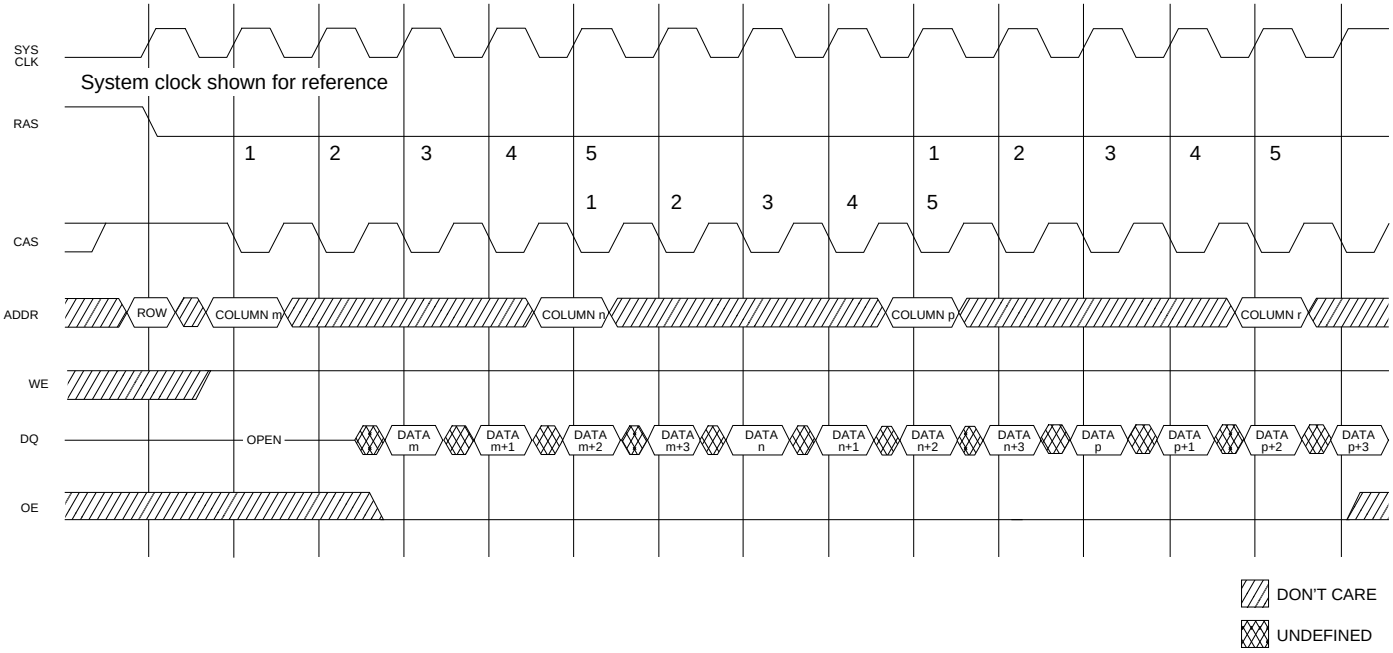

Figure 1
CONTINUOUS BURST OPERATION

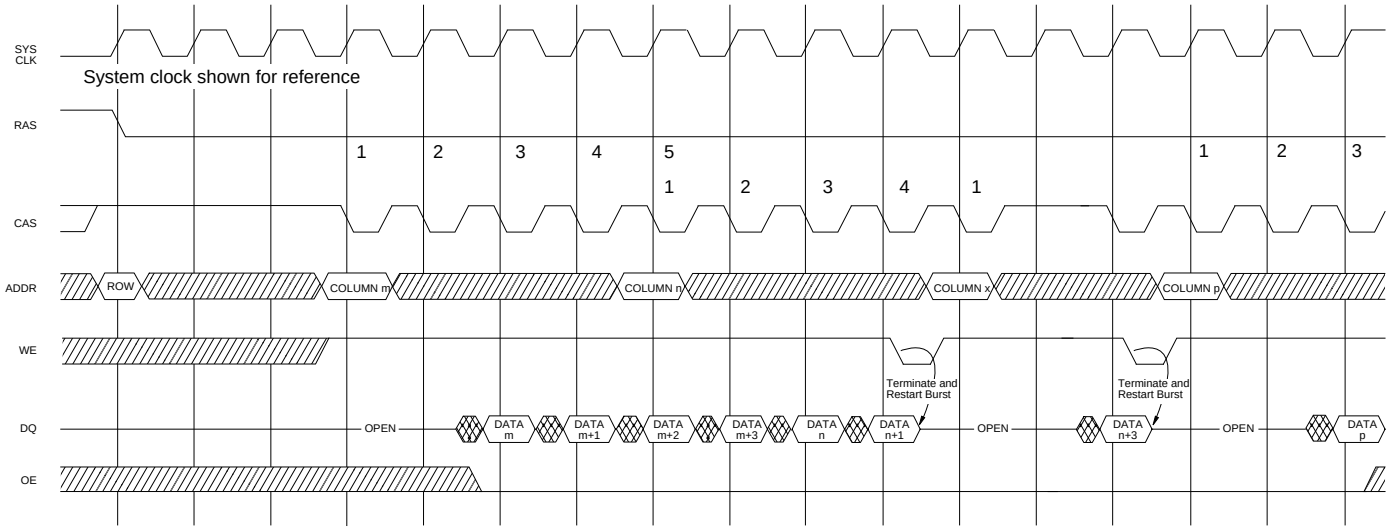

Figure 2
READ, TERMINATE, READ OPERATION

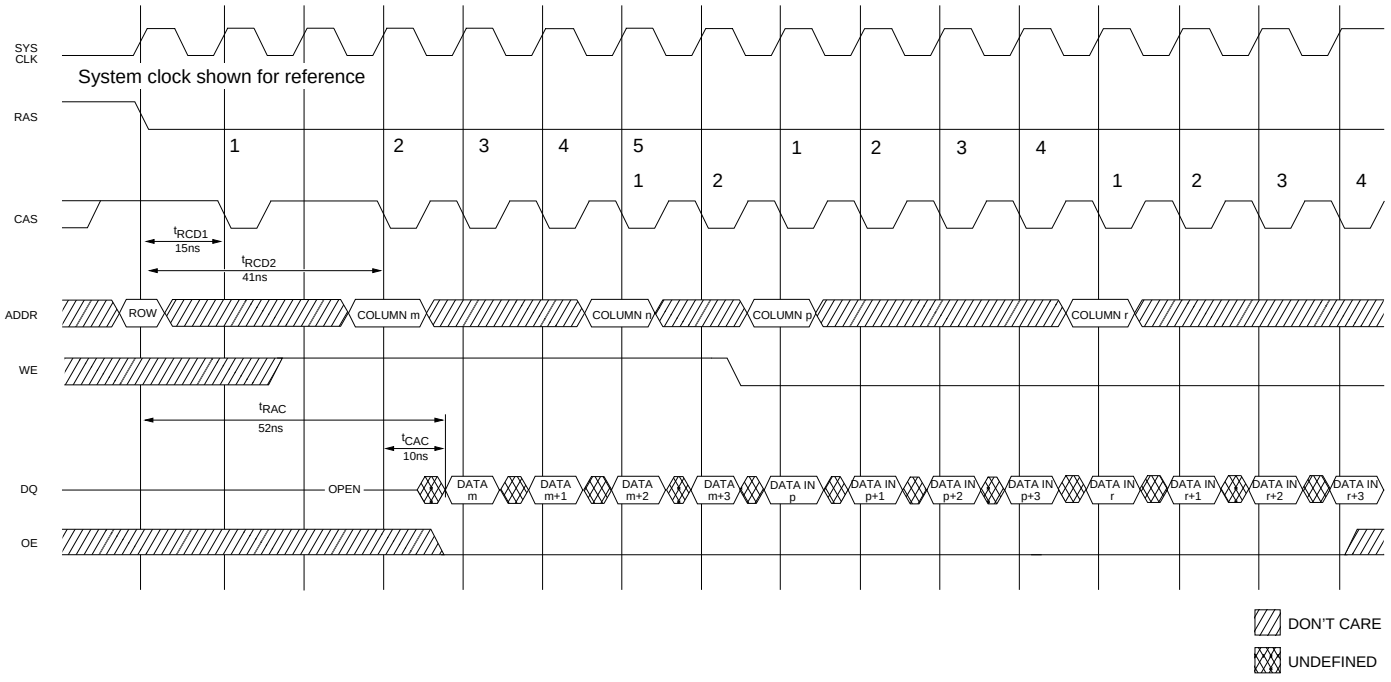

Figure 3
BURST READ, BURST WRITE OPERATION

data after which each $\overline{CAS}$ cycle delivers data. However, the first $\overline{CAS}$ may be "hidden" during the ^tAA time required by FPM and EDO DRAMs. That is, the first $\overline{CAS}$ cycle occurs during the ^tRAC time of FPM and EDO DRAMs. Burst EDO DRAMs have the same lead-off access time as EDO DRAMs. This exposed pipeline occurs only when there are idle cycles between READ burst cycles (terminating a burst READ) or going from a WRITE to a READ operation. See Figures 2 and 4 respectively.

Opening a page ($\overline{RAS}$ transitions from inactive to active) also requires the extra $\overline{CAS}$ pulse but the pipeline is not exposed since the extra $\overline{CAS}$ cycle is hidden by the ^tRAC access time. (See Figure 3.)

The pipeline is not exposed, i.e., continuous data-in-and-out for all WRITE operations, transitioning from a READ to a WRITE, and continuous READ operations. These cycles are illustrated in Figures 3 and 1 respectively.

PERFORMANCE OF BURST EDO

Burst EDO was designed to achieve zero wait-state performance at 66 MHz and beyond. Currently FPM and EDO DRAMs achieve zero wait-state performance at 28 MHz and 40 MHz respectively. Thus BEDO was designed to deliver zero wait-state operation at the PC bus frequencies being used in mainstream desktop and portable applications for the next several years. Burst EDO achieves a 100 percent increase in performance over FPM and a 33 to 50 percent increase over EDO DRAMs. Table 1 compares FPM, EDO and Burst EDO maximum frequencies for zero wait-state performance.

Sixty-six MHz frequency is not the limit of BEDO but the near-term target for zero wait-state operation. The current -5 specification, while calling out ^tPC or 15ns (66 MHz), indicates that Burst EDO is capable of running faster (^tCAS + ^tCP) which equates to 100 MHz (5 + 5) or 10ns. Micron is currently cycling -5 BEDO at 125 MHz (3.0V and 85°C). However, Micron believes that the -5 specification is what is needed for a 66 MHz system bus.

Table 1
MAXIMUM ZERO WAIT-STATE FREQUENCIES

DRAM SPEED (^tRAC)	DRAM TYPE		
	FAST PAGE MODE	EDO	BURST EDO
70ns	25 MHz	33 MHz	50 MHz
60ns	28 MHz	40 MHz	60 MHz
50ns	33 MHz	50 MHz	66 MHz

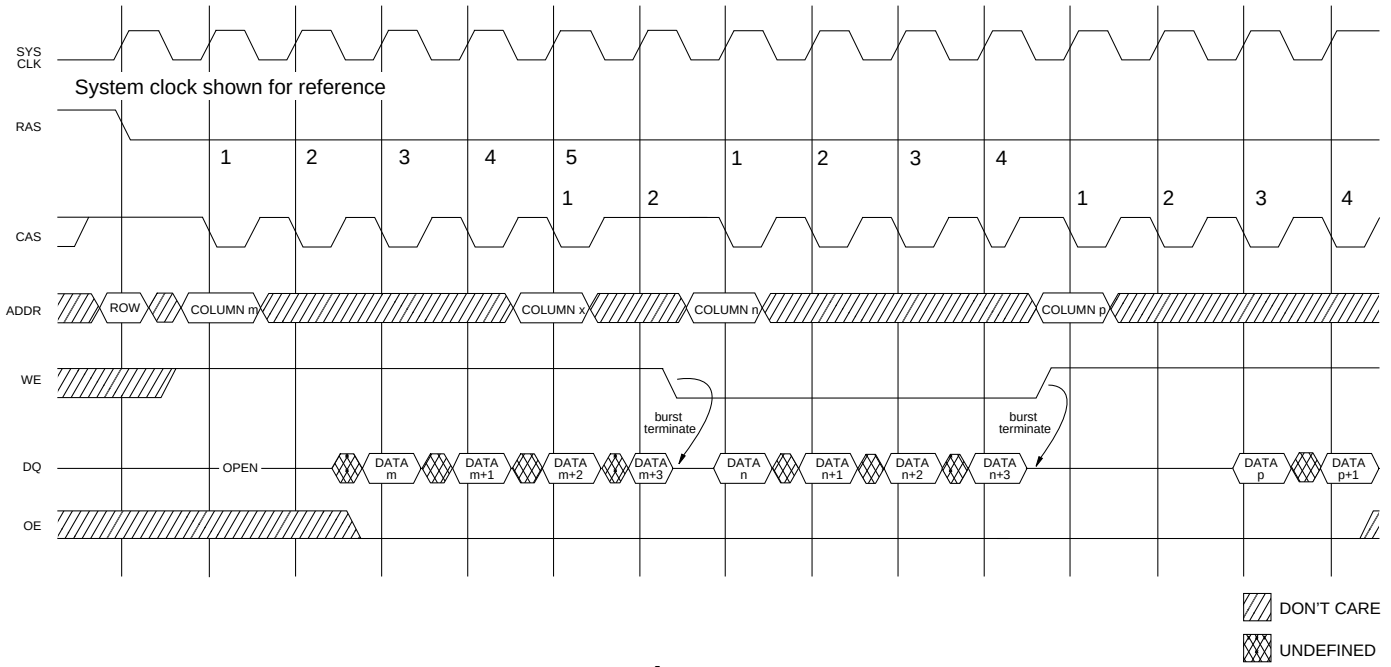

Figure 4
READ BURST, BURST WRITE OPERATION

Unlike BEDO, the SDRAM specifications advertise cycle times which, when looking closer, would require wait states to operate at the advertised frequencies. Cycling fast is of no consequence if wait states are required at the specified frequency. Table 2 compares the critical specifications of Burst EDO DRAMs and SDRAMs at 66 MHz operation.

As seen in Table 2, a -10 (100 MHz) SDRAM with a $\overline{CAS}$ latency of 3 is required for zero wait-state operation at 66 MHz. By contrast the BEDO -5 (66 MHz) part has a specification that allows zero wait-state operation at the specified -5 cycle rate of 66 MHz. The SDRAM -10 specifications also require an extra lead-off cycle over BEDO for all READ operations ($\overline{CAS}$ latency of 3) to achieve the -5 BEDO ^{t}CAC specification. This specification is critical to zero wait-state operation. Another major difference between BEDO and SDRAM is that the manufacturers of BEDO DRAMs all have very similar timings while SDRAM timing specifica

Table 2
BURST EDO DRAM AND SDRAM DATA SHEET COMPARISON

PARAMETER	MICRON BURST EDO		BEST SDRAM SPEC		LEAST COMMON DENOMINATOR FROM SEVERAL SDRAM SPECS		66 MHz DESIGN
Speed Grade	-5	-6	-10	-12	-10	-12	
Advertised Operating Frequency (MHz)	66.6	60	100	83.3	100	83.3	66.6
Cycle Time (^{t}PC/^{t}CK)	15	16.6	10	12	10	12	15
^{t}RAC	52	60	53	61	57	61	55 or less
Access Time from $\overline{CAS}$/Clock							
^{t}CAC/^{t}CKA (latency = 2)	10	11.6	13	14	13	15	10 or less
^{t}CAC/^{t}CKA (latency = 3)	10	11.6	8.5	9	10	12	10 or less
Output Data Hold (^{t}COH/^{t}OH)	3	3	4	4	3	3	3 or more
Time for System Delay (^{t}PC - ^{t}CAC)/(^{t}CK - ^{t}CKA)							
latency = 2	5	3.4	2	1	2	0	3 or more
latency = 3	20	18.4	6.5	6	5	3	3 or more
Data Out Window (^{t}PC-^{t}CAC+^{t}COH)/(^{t}KC-^{t}CKA+^{t}OH)							
latency = 2	8	8	6	5	5	3	5 or more
latency = 3	23	21.4	6.5	6	5	3	5 or more
66 MHz Lead-off Clocks (page miss)							
latency = 2	6	7	6	7	6	7	
latency = 3	6	6	7	8	7	8	
66 MHz Lead-off Clocks (page hit)							
latency = 2	2	3	2	2	2	2	
latency = 3	2	3	3	3	3	3	
66 MHz Burst Clocks							
latency = 2	1	2	2	2	2	2	
latency = 3	1	2	1	1	1	2	

Useable at 66 MHz for 0ws operation
Marginal at 66 MHz for 0ws operation
Unusable at 66 MHz for 0ws operation

tions vary greatly from vendor to vendor. To use multiple manufacturers' SDRAM devices, a design would have to incorporate the least common denominators of all vendors' specifications. Table 3 shows the wide variation between SDRAM manufacturers' data sheets along with the least common denominator of those shown.

SUMMARY

Burst EDO is an evolutionary approach to achieve higher performance from the fundamental standard DRAM architecture. BEDO was implemented on the same die as FPM and EDO DRAMs. BEDO uses the same pinout, packages, and modules as FPM and EDO. These concepts make BEDO producible at the same cost as EDO and FPM devices. Burst EDO delivers twice the performance of FPM DRAMs, about 40 percent more performance than EDO DRAMs, and better performance when compared to the SDRAM for 66 MHz operation. Burst EDO is positioned to be the next low-cost, main memory standard after EDO DRAMs. The support BEDO has already received from other DRAM manufacturers, chipset manufacturers, systems manufacturers and JEDEC standardization, attests to the fact that BEDO is well on its way to becoming the next industry standard for PC main memory.

Table 3
SDRAM SPECIFICATION COMPARISON

PARAMETER	SDRAM A		SDRAM B		SDRAM C		SDRAM D		LEAST COMMON DENOMINATOR FROM SEVERAL SDRAM SPECS	
Speed grade	-10	-12	-10	-12	-10	-12	-10	-12	-10	-12
^{t}RAC	60	72	53	61	57	69	58	69	53	72
Access time from $\overline{\text{CAS}}$/Clock										
^{t}CKA (latency = 2)	12.5	15	13	14	12	15	13	15	13	15
^{t}CKA (latency = 3)	10	12	8.5	9	9	11	8	10	10	12
Output data hold (^{t}OH)	5	5	4	4	4	4	3	3	3	3
^{t}RP	46	30	38	30	36	30	36	40	46	40
Refresh (2K/4K)	4K	4K	4K	4K	2K	2K	4K	4K	2K & 4K	2K & 4K
Data-in setup	2	2	3	3.5	3	3.5	2	3	3	3.5
Data-in hold	3	4	1	1.5	1	1.5	1	1	1	1